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Design and Analysis for Removing Salt and Pepper Noise in Image Processing

¹F.M. Aiysha Farzana, ²Hameedhul Arshadh. A, ³Sara Safreen. M, ⁴Dr. N. Muthukumaran & ⁵Dr. Vinod Varma Vegesna

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AB ST R ACT

In this project, an efficient method is proposed to remove the high level of salt and pepper noise in image using median filter. The objective of any noise removal technique is to remove the noise completely from the image, such that the resulting image is better than original image. Salt and pepper noise can be added to image during acquisition process. This noise is removed by the proposed method. This plays a vital role in digital images. The proposed approach is used to improve the quality of the image by removing high tone salt and pepper noise. The time consumption for removing salt and pepper noise in image can be reduced in this approach. The verification is based on filtered images. The resultant image is the converted into binary code. Then the binary code of the resultant image is simulated in Xilinx software. Then it is implemented in FPGA kit using Xilinx software. The resultant image will have good noise removal efficiency.

Keywords: Image Processing, MATLAB, VLSI, Noise, Implementation, Xilinx.

1. INTRODUCTION

An image is an art that depicts visual perception that has a similar appearance to some physical object or a person, thus providing a depiction of it. Images may be two-dimensional such as a statue or hologram. They are captured by optical devices such as cameras, mirrors, lenses, telescopes, microscopes, etc. and natural objects and phenomena such as human eye or water. In this wider sense, images can also be rendered manually such as by drawing, the art of painting, carving, rendered automatically by printing or computer graphics technology, or developed by a combination of methods, especially in a pseudo-photograph. A volatile image is one that exists only for a short period of time. This may be a reflection of an object by a mirror, a projection of a camera observation, or a scene displayed on a cathode ray tube. A fixed image, also called a hard copy, is one that has been recorded on a material object such as paper or textile by photography or any other digital process. The major problem occurred in image is noise. Noise can be added in image during acquisition process. Image acquisition is defined as the action of retrieving an image from some source, usually a hardware based source, so it can be passed through whatever processes need to occur afterward. Performing image acquisition in image processing is always the first step in the workflow sequence because, without an image, no processing is possible.

2. EXISTING SYSTEM

The image is given as input to MATLAB. Then it is converted into binary image using codes. The pixels of image are overlapped using simulink and system generator is used to remove salt and pepper noise in image using various filters such as median filter, Gaussian filters. The resultant image is viewed by using FPGA kit. If improvement is needed, the image is again given to mat lab and simulink to remove salt and pepper noise and improve quality of the image. This process is looking like a loop process. This is continued until all noise was removed.

The image is read in Mat lab and then it is given to Xilinx system generator via simulink in Mat lab. The noise is reduced in this Xilinx system generator. Then it is implemented in FPGA by using Xilinx system generator. The output image shows good trade-off between resource consumption and noise removal efficiency [1-11].

^{1, 2, 3}UG Student, ⁴Professor, ⁵Sr. IT Security Risk Analyst,

^{1,2,3,4} Department of ECE, Francis Xavier Engineering College, Tirunelveli-627003, Tamilnadu, India.

⁵ The Auto Club Group, United States of America.



3. PROPOSED SYSTEM

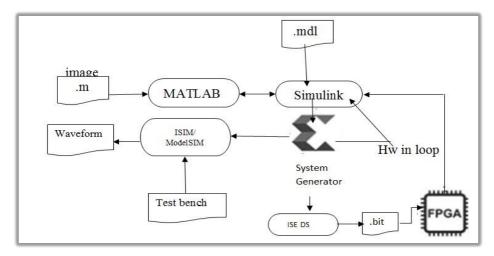


Fig.1: Block Diagram of Existing System

3.1 Introduction

Digital images are highly corrupted by salt and pepper noise while during acquisition and enhancement process. So quality of image is decreased. Further processing of an image for its enhancement needs this salt and pepper noise to be removed, otherwise performance of image processing tasks such as segmentation, feature extraction, object recognition, etc. are severely degraded by salt and pepper noise. So we concentrate on removing salt and pepper noise in image and implementation of such a result image in FPGA.

3.2 SALT and PEPPER NOISE

Salt and pepper noise otherwise called as impulsive or distributed noise. They are formed in image while capturing image. They are present in image during acquisition process of analog form conversion to digital form. They may be formed by hardware limitations, processing delays, blurring occurs in cameras. Small and sharp white and black dots are formed in image and they are called as salt and pepper noise.

3.3 NOISE REDUCTION TOOLS

Now a day, there are many tools used to remove noise in image. Here we uses the software tools are Mat lab and Xilinx. The hardware used to implement the resultant image is FPGA.

3.4 PROCESS:

3.4.1 Reading Image:

The input image can be read in Mat lab using the syntax: I=imread ("filename.format");

The image can be showed by using the syntax: Imshow (I);

3.4.2 ADDITION OF NOISE:

The salt and pepper noise can be added into the input image by using the syntax:

J=imnoise (,,I, salt & Pepper, d");

Where, I is input image and d is density of noise to be added.

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3.4.3 SIMULINK PROCESS:

The simulink contains several blocks to remove noise in image [12-31]. The noisy image can be read from workspace of Mat lab using "Image from workspace" block. The parameters given for this block are: Input image name and type of image (one dimensional or RGB model).

4. RESULT AND DISCUSSION

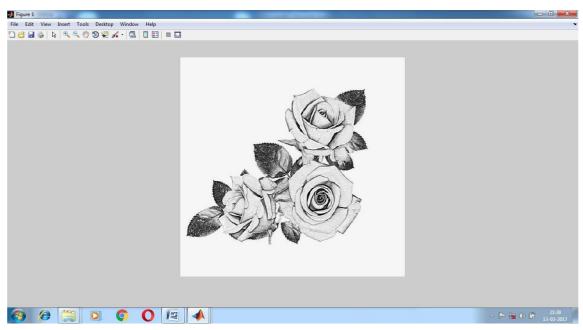


Fig 2: Input Image Read in MAT LAB.

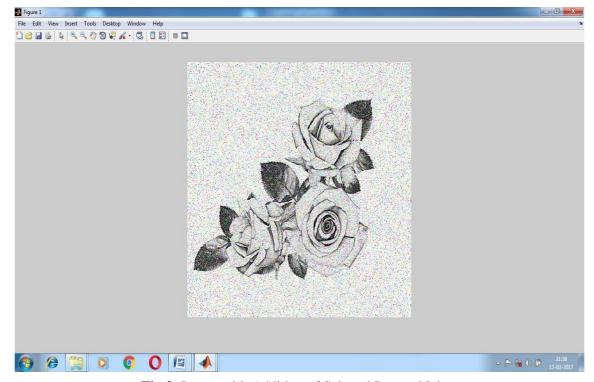


Fig 3: Image with Addition of Salt and Pepper Noise.



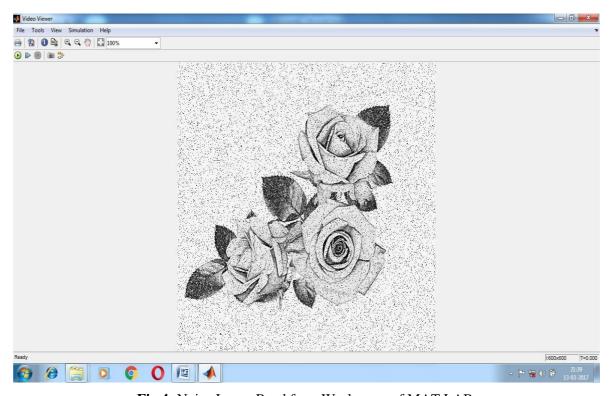


Fig 4: Noisy Image Read from Workspace of MAT LAB.

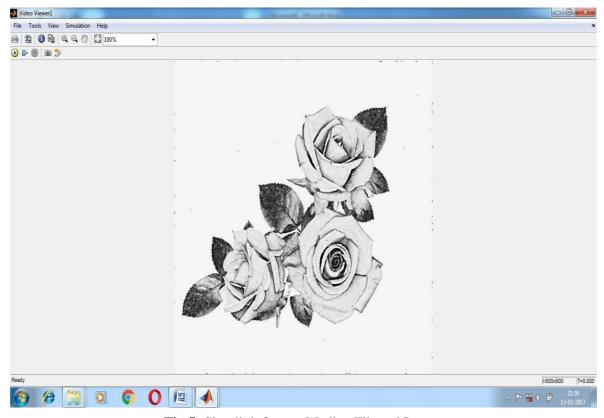


Fig 5: Simulink Output Median Filtered Image.

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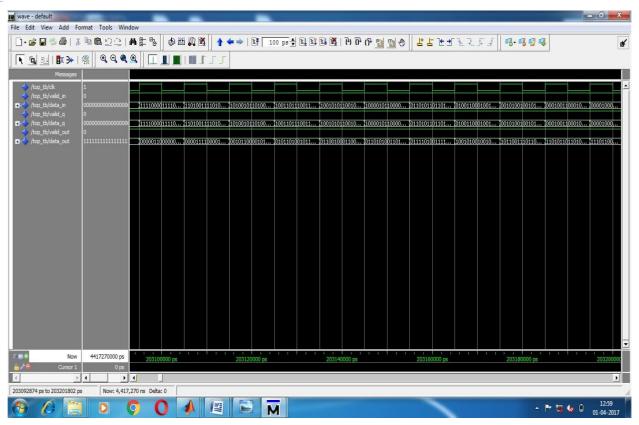


Fig 6: Modal-sim Output

5. CONCLUSION

Here we conclude that the existing system having disadvantages of decrease in quality, decrease in noise removal efficiency. These drawbacks are overcome by our proposed system. In our project salt and pepper noise are removed efficiently. The quality of image is increased by removing salt and pepper noise. The high tone salt and pepper noise also removed by median filter. The resultant image shows good trade-off between resource consumption. The resultant image is implemented in FPGA.

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